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Vladimir Voevodin · Sergey Sobolev (Eds.)

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6th Russian Supercomputing Days, RuSCDays 2020 Moscow, Russia, September 21–22, 2020 Revised Selected Papers



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Preface

The 6th Russian Supercomputing Days Conference (RuSCDays 2020), was held during September 21–22, 2020. The conference was dedicated to the 65th anniversary of the Research Computing Center, Moscow State University (RCC MSU) and the 100th anniversary of I.S. Berezin, the first RCC MSU director.

The conference was organized by the Supercomputing Consortium of Russian Universities and the Russian Academy of Sciences. The conference organization coordinator was RCC MSU.

Due to COVID-19 pandemic, for the first time the conference was held online. It was a new challenge for the conference organizers. However, online format provides a number of opportunities which are hard to perform offline, e.g. gathering invited speakers from all around the world. At the same time, the Organizing Committee did its best to keep the look and feel of the real-life meeting for attendees, including traditional sets of conference events – sessions, workshops, exhibitions, etc.

The conference was supported by the Russian Foundation for Basic Research and our respected partner (IBM), platinum sponsors (RSC, Merlion, Hewlett Packard Enterprise, Intel, Huawei), gold sponsors (NVIDIA, Dell Technologies in a partnership with CompTek), and silver sponsor (Xilinx). The conference was organized in a partnership with the ISC High Performance conference series.

RuSCDays was born in 2015 as a union of several supercomputing event series in Russia and quickly became one of the most notable Russian supercomputing international meetings. The conference caters to the interests of a wide range of representatives from science, industry, business, education, government, and students – anyone connected to the development or the use of supercomputing technologies. The conference topics cover all aspects of supercomputing technologies: software and hardware design, solving large tasks, application of supercomputing technologies in industry, exaflops-scale computing issues, supercomputing co-design technologies, supercomputing education, and others.

All 106 papers submitted to the conference were reviewed by three referees in the first review round. During single-blind peer reviewing, the papers were evaluated according to their relevance to the conference topics, scientific contribution, presentation, approbation, and related works description. After notification of conditional acceptance, the second review round arranged aimed at the final polishing of papers and also at the evaluation of authors' work after the referees' comments. After the conference, the 55 best papers were carefully selected to be included in this volume.

The proceedings editors would like to thank all the conference committees members, especially the Organizing and Program Committee members as well as the referees and reviewers for their contributions. We also thank Springer for producing these high-quality proceedings of RuSCDays 2020.

October 2020

Vladimir Voevodin Sergey Sobolev

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Resource-Efficient Parallel CG Algorithms for Linear Systems Solving on Heterogeneous Platforms

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Abstract. The article discusses the parallel implementation of solving systems of linear algebraic equations on the heterogeneous platform containing a central processing unit (CPU) and graphic accelerators (GPU). The performance of parallel algorithms for the classical conjugate gradient method schemes when using the CPU and GPU together is significantly limited by the synchronization points. The article investigates the pipeline version of the conjugate gradient method with one synchronization point, the possibility of asynchronous calculations, load balancing between the CPU and GPU when solving the large linear systems. Numerical experiments were carried out on test matrices and computational nodes of different performance of a heterogeneous platform, which allowed us to estimate the contribution of communication costs. The algorithms are implemented with the combined use of technologies: MPI, OpenMP and CUDA. The proposed algorithms, in addition to reducing the execution time, allow solving large linear systems, for which there are not enough memory resources of one GPU or a computing node. At the same time, block algorithm with the pipelining decreases the total execution time by reducing synchronization points and aggregating some messages in one.

Keywords: Parallel computing on heterogeneous platform \cdot Hybrid parallel technologies \cdot Conjugate gradient method \cdot Reduction of communications

1 Introduction

Computing accelerators are contained in the computing nodes of supercomputers and are used quite successfully in solving many computing problems despite the fact that the central processor (CPU) is idle after running the core functions on the accelerator. There are several more important conditions for which the

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joint use of the CPU and accelerators (for example, GPU) in parallel computing within the same problem seems to be promising.

Each architecture of the CPU and GPU has unique features and, accordingly, is focused on solving certain tasks for which typical, for example, high performance or low latency. Heterogeneous nodes containing and sharing CPU plus GPUs can provide an effective solution to a wide range of problems or one problem for which the parallel properties of the algorithms are changed and determined to be executed on one or another computing device. We also note the high energy efficiency of the heterogeneous computing systems.

One of the computationally complex operations in numerical methods is the solution of linear systems (SLAE). Currently, many parallel algorithms have been proposed that provide high performance and scalability when solving large sparse systems of equations on modern multiprocessor with a hierarchical architecture.

The construction of hybrid solvers with a combination of direct and iterative methods for solving SLAE allows the use of several levels of parallelism [1–5]. So in [6] a hybrid method for solving systems of equations of Schur complement by preconditioned iterative methods from Krylov subspaces was built and implemented when used together the cores of central (CPU) and graphic processing units (GPU). The classical preconditioned conjugate gradient method [7] was applied for the block ordered matrix and the separation of calculations in matrix operations between the CPU and one or more GPUs, when the system of equations in Schur complement was solved in parallel.

Currently, there are several approaches for computing load scheduling of the parallel conjugate gradient method (CG) on heterogeneous Multi-CPUs/Multi-GPUs platforms. Firstly, the separate steps of the CG algorithm are executed on a CPU or GPU, such as a preconditioner [8].

Second approach is based on the data mapping (matrix block and vectors) or separate tasks are carried out of all CG steps on the CPU or GPU [6].

In [9] task scheduling on Multi-CPUs/Multi-GPUs platforms for the classical CG from the PARALUTION library is executed in the StarPU. It's unified runtime system for heterogeneous multicore architectures which is developed in the INRIA laboratory (France).

In this paper, we consider an approach that reduces the cost of data exchanging between the CPU and GPU by reducing the number of synchronization points and pipelining of computing when SLAE is solved on heterogeneous platforms.

The Krylov subspace methods are some of the most effective options for solving large-scale linear algebra problems. However, the classical Krylov subspace algorithms do not scale well on modern architectures due to the bottleneck related to synchronization of computations. Pipeline methods of the Krylov subspace [10] with hidden communications provide high parallel scalability due to the global communications overlapping with computing, performing matrixvector and dot products. The first work on reducing communications was related to a variant of the conjugate gradient method, having one communication at each iteration [11], using the three-term recurrence relations CG [12].

The next stage of development was the emergence of s-step methods from Krylov subspaces [13], in which the iterative process in the s-block uses various bases of Krylov subspaces. As a result, it was possible to reduce the number of synchronization points to one per s iterations. However, for a large number of processors (cores), communications can still take significantly longer than computing a single matrix-vector product. In [14] it was proposed a CG algorithm using auxiliary vectors and transferring a sequential dependence between the computing of matrix-vector product and scalar products of vectors. In this approach, the latency of communications is replaced by additional calculations.

2 Pipelined Algorithm of the Conjugate Gradient Method

We consider now the pipelined version of the conjugate gradient method, which is mathematically equivalent to the classical form of the preconditioned CG method and has the same convergence rate.

Algorithm 1: Pipelined algorithm CGwO.

 $1 \ r = b - Ax;$ **2** $u = M^{-1}r;$ **3** w = Au;4 $\gamma_1 = (r, u); \, \delta = (w, u);$ while $||r||_2 / ||b||_2 > \varepsilon$ do $m = M^{-1}w ;$ 5 6 n = Am;if (j = 0) then 7 else $\beta = \gamma_1 / \gamma_0 ;$ 8 $\alpha = \gamma_1 / (\delta - \beta \gamma_1 / \alpha) ;$ 9 $z = n + \beta z; w = w - \alpha z; s = w + \beta s; r = r - \alpha s;$ 10 $p = u + \beta p; x = x + \alpha p; q = m + \beta q; u = u + \alpha q;$ 11 12 $\gamma_0 = \gamma_1;$ $\gamma_1 = (r, u); \, \delta = (w, u);$ 13

In this algorithm, the modification of the vectors r_{j+1} , x_{j+1} , s_{j+1} , p_{j+1} and matrix-vector products provides pipeline computations. The computation of dot products (line 4) can be overlapped with the computation of the product by the preconditioner (line 3) and the matrix-vector product (line 3). However, the number of triads in the algorithm increases to eight, in contrast to three for the classic version and four in [13]. In this case, a parallel computation of triads and two dot products at the beginning of the iterative process and one synchronization point is possible. The pipelined version CG presented in this work can be used with any preconditioner. There are two ways to organize computations in the preconditioned pipelined CG, which provide a compromise between scalability and the total number of operations [15]. Thus, the CG pipeline scheme is characterized by a different order of computations, the presence of global communication, which can overlap with local computations, such as matrix-vector product and operations with a preconditioner, and the possibility of organizing asynchronous communications.

The two variants of the conjugate gradient method were compared: the classical scheme and the pipelined one. Table 1 presents the results of numerical experiments where the execution time of a sequential version of the classical CG and the CGwO pipelined scheme (Algorithm 1) executed on the CPU and GPU are shown. Note that in the variants for the GPU, joint computation of all dot products of vectors in one kernel function was implemented, independently of each other. For this, when starting the CUDA kernel, the dimension of the Grid hierarchy of CUDA threads was set in two-dimensional form: 3 sets of blocks, each for performing computations on its own pair of vectors. This allowed us to reduce the number of exchanges between the CPU and GPU memory, combining all the resulting scalars in one communication.

Matrices from the SuiteSparse Matrix Collection (formerly the University of Florida Sparse Matrix Collection, https://sparse.tamu.edu/) were used in the test computations. The right hand side vector was formed as a row-wise sum of matrix elements. Thus, the solution of the system Ax = b, dimension $N \times N$ (with the number of nonzero elements nnz) is a vector $x = (1, 1, ..., 1)^T$.

For systems of equations of small dimension, the solution time on the CPU according to the classical CG scheme is significantly less than the GPU execution time for the same number of iterations (see Table 1). For large systems, the costs of synchronization and forwarding between the CPU and GPU overlap with the speed of the GPU. In the pipelined version of CGwO, the computational execution costs on the GPU are reduced almost threefold for all the considered systems of equations only due to the reduction of exchanges between the GPU and the CPU in the computation of dot products.

3 CG with the Combined Use of CPU and GPU

Let us consider the application of the Algorithm 1 for the parallel solution of super-large systems of equations on computing nodes, each of which contains several CPUs and GPUs. To solve SLAEs on several GPUs, we construct a block pipelined algorithm for the conjugate gradient method. On heterogeneous platform, data exchange between different GPUs within the same computing node is carried out with OpenMP technology, and the exchange between different computing nodes is carried out by MPI technology.

For example, consider a node containing a central eight-core processor and two graphics accelerators. The number of OpenMP threads is selected by the number of available CPU cores. The first two OpenMP threads are responsible

for exchanging data and running on two GPUs. Threads 2–6 provide computations on the CPU and can perform computations on a block of the SLAE matrix. The last thread provides data exchange with other computing nodes by MPI.

3.1 Matrix Partitioning

To divide the matrix A into blocks, we construct the graph $G_A(V, E)$, where $V = \{i\}$ is the set of vertices associated with the row index of the matrix (the number of vertices is equal to the number of rows of the matrix A); $E = \{(i, j)\}$ is the set of edges. Two vertices i and j are considered to be connected if the matrix A has a nonzero element with indices i and j. The resulting graph is divided into subgraphs whose number is d. For example, to split a graph, you can use the [16] layer-by-layer partitioning algorithm, which reduces communication costs due to the need to exchange only with two neighboring computing nodes. After that, each vertex of the graph is assigned its own GPU or CPU. On each computing unit, the vertices are divided into internal and boundary. The latter are connected with at least one vertex belonging to another subgraph.

After partitioning, each block A_k of the original matrix A contains the following submatrices:

 $-A_k^{[i_k,i_k]}$ – matrix associated with the internal vertices; $-A_k^{[i_k,b_k]}, A_k^{[b_k,i_k]}$ – matrices associated with the internal and boundary vertices; $-A_k^{[b_k,b_l]}$ – matrix associated with the boundary vertices of the k-th and l-th blocks

Then the matrix A can be written in the following form:

$$A = \begin{pmatrix} A_1^{[i_1,i_1]} & A_1^{[i_1,b_1]} & \cdots & 0 & 0\\ A_1^{[b_1,i_1]} & A_1^{[b_1,b_1]} & \cdots & 0 & A_1^{[b_1,b_d]}\\ \vdots & \vdots & \ddots & \vdots & \vdots\\ 0 & 0 & \cdots & A_d^{[i_d,i_d]} & A_d^{[i_d,b_d]}\\ 0 & A_d^{[b_d,b_1]} & \cdots & A_d^{[b_d,i_d]} & A_d^{[b_d,b_d]} \end{pmatrix}$$

We divide the matrix-vector product n = Am into two components by using the obtained partition:

$$n_k^b = A_k^{[b_k, i_k]} m_k^i + \sum_{l=1}^{l \le d} A_k^{[b_k, b_l]} m_l^b, \qquad n_k^i = A_k^{[i_k, i_k]} m_k^i + A_k^{[i_k, b_k]} n_k^b.$$
(1)

Here k corresponds to the computing device. The block representation of the vectors involved in the algorithm is inherited from the matrix partitioning. For example, the vector m has the form $m^T = (m_1^i, m_1^b, \ldots, m_k^i, m_k^b, \ldots, m_d^i, m_d^b)$. The implementation of the matrix-vector product reduces the cost of communication between blocks at each iteration of conjugate gradient method. To perform this operation, an exchange of vectors m_k^b is required, the size of which is less than the dimension of the initial vector m.

The partitioning of the preconditioner M is carried out in a similar way.

3.2 Block Pipelined Algorithm

The matrix blocks were mapped on the available CPU and GPU with the block partitioning of the matrix and vectors. The number and size of blocks let on to map the load in accordance with the performance of the computing units, including the allocation of several blocks to one.

Algorithm 2: Block algorithm CGwO performed on k-th device

	Data: Matrix partitioning into blocks $A_k^{[i_k,i_k]}$, $A_k^{[i_k,b_k]}$, $A_k^{[b_k,i_k]}$, $A_k^{[b_k,b_l]}$.						
1	Data. Matrix partitioning into blocks A_k , A_k , A_k , A_k , A_k . 1 $r = b$;						
	u = 0, $u = M^{-1}r;$						
-	// Parallel algorithm branches						
	// $(CPU \lor GPU)_k$ // CPU						
9	$\mathbf{a} w_k^i = A_k^{[i_k, i_k]} \cdot u_k^i + A_k^{[i_k, b_k]} \cdot u_k^b; \text{Assembly of the vectors } u_k^b;$						
	$ \begin{split} & w_k = A_k & u_k + A_k & u_k, \\ & w_k^b = A_k^{[b_k, b_k]} \cdot u_k^b + A_k^{[b_k, i_k]} \cdot u_k^i; & w_h^b = \sum_{l=1, l \neq k}^{l \leq d} A_k^{[b_k, b_l]} \cdot u_k^b; \end{split} $						
5	Copying w_h^b on the GPU_k ;						
	$w_k^b = w_k^b + w_h^b;$						
	$m = M^{-1}w;$ Assembly of the vectors $m_k^b;$						
8	8 $\gamma_{1k} = (r_k, u_k); \ \delta_k = (w_k, u_k);$ Assembly $\delta = \sum_k \delta_k; \gamma_1 = \sum_k \gamma_{1k};$						
	while $ r _2/ b _2 > \varepsilon$ do						
9	$n_{k}^{i} = A_{k}^{[i_{k}, i_{k}]} \cdot m_{k}^{i} + A_{k}^{[i_{k}, b_{k}]} \cdot m_{k}^{b}; n_{h}^{b} = \sum_{l=1, l \neq k}^{l \leq d} A_{k}^{[b_{k}, b_{l}]} \cdot m_{k}^{b};$						
10	$n_{k}^{b} = A_{k}^{[b_{k}, b_{k}]} \cdot m_{k}^{b} + A_{k}^{[b_{k}, i_{k}]} \cdot m_{k}^{i}; \text{ Copying } n_{h}^{b} \text{ on the } \operatorname{GPU}_{k};$						
10	$m_k - A_k$ $m_k + A_k$ m_k , Copying n_h^o on the GPU _k ;						
	$n_{h}^{b} = n_{h}^{b} + n_{h}^{b};$ $\beta - ((i - 0)?0 + \gamma_{1}/\gamma_{2});$						
12 13	$\kappa - \kappa - n^{2} - ((J - 0) \cdot 0 \cdot (J - 1))),$						
13 14	$ \begin{array}{l} z = n + \beta z; \\ w = w - \alpha z; \end{array} \qquad \qquad \alpha = \gamma_1 / (\delta - \beta \gamma_1 / \alpha); \\ \end{array} $						
14	$a = a + \beta a;$ $a = m + \beta a;$						
16							
17	$s = w + \beta s;$ $p = u + \beta p;$ Assembly of the vectors $w_k^b;$						
18	$x = x + \alpha p;$						
19	$r = r - \alpha s;$ Asymptotic vectors m^b .						
20	$ \begin{array}{l} r = r - \alpha s; \\ u = u + \alpha q; \end{array} \qquad \qquad \text{Assembly vectors } m_k^b; \\ \end{array} $						
21	$m = M^{-1} \widetilde{w}; \qquad \text{Assembly } \delta = \sum_k \delta_k; \gamma_1 = \sum_k \gamma_{1k};$						
22							
23	$ \gamma_{1k} = (r_k, u_k); \delta_k = (w_k, u_k); $						

Let us represent parallel block scheme of the method CGwO that is performed each k-th computing unit in the form of Algorithm 2. Two parallel branches of this algorithm are executed accordingly on the CPU and GPU/CPU. Operations performed in parallel are shown in one line of the algorithm. Vector operations on each computing unit occur in two stages, for internal and boundary nodes. The designations of the internal and boundary nodes for vectors are omitted, with the exception of the matrix-vector multiplication. Dot products are performed independently by each computing unit on its parts of vectors. The summation

of intermediate scalars occurs in parallel threads responsible for communication, which is the synchronization point at each iteration of the algorithm.

In block CGwO, compared to Algorithm 1, the preconditioning step has been moved (line 5 to line 21). This is done in order to combine vector operations on the computing unit and the assembly of the vector parts of the right hand side to perform matrix-vector multiplication in preconditioning. The 13 line on the right uses the ternary operator: if j = 0, then $\beta = 0$, in other cases $\beta = \gamma_1/\gamma_0$. The subscript *h* is used for vectors that are stored only in CPU memory.

Numerical experiments on the Algorithm 2 were carried out on heterogeneous platform with various configuration of computing nodes containing several CPUs and GPUs. In the general case, the parallel computing on several heterogeneous computing nodes containing one or more CPUs and several GPUs is implemented by the combination of several technologies: MPI, OpenMP and CUDA.

Let us consider the software organization of computations using as example some cluster, which includes two computing nodes (8 CPU cores and 2 GPUs). Each computing node is associated with a parallel MPI process. In a parallel process, 9 parallel OpenMP threads are generated, which is one more than the available CPU cores. The eighth OpenMP thread is responsible for communications between different computing nodes (using MPI technology, vector assembly using the Allgatherv function, adding scalars Allreduce) and various GPUs. In the 2 Algorithm, the operations performed by this thread are presented to the right. Zero and first OpenMP threads are the host threads for one of the available GPU devices and are responsible for transfer data between the GPU-CPU (calls to asynchronous copying functions) and auxiliary computations. Each available GPU device (further considered as a computing unit) is associated with one of the parallel OpenMP threads, which is responsible for transferring data between the GPU and CPU (calls to asynchronous copy functions) and participates with the eighth treads in matrix-vector product on boundary vertices (lines 4, 9 right column). The remaining parallel threads (second to seventh) perform the calculations as a separate computing unit for their matrix block. The operations performed by computing units in the 2 Algorithm are shown on the left.

The preconditioning in lines 2, 7 and 21 implies the use of block matrix-vector multiplication of the form (1) considered above.

4 Numerical Experiments

The numerical experiments were performed on the heterogeneous partitions of cluster "Uran" on the computing nodes (CNs) of several types of Supercomputer center IMM UB RAS, Yekaterinburg, Russia. The cluster partitions with the following characteristics were used:

- partition "debug": 4 CNs tesla [31–32,46–47] with two 8-cores CPU Intel Xeon E5-2660 (2.2 GHz), cache memory is 20 MB L3 cache, RAM is 96 GB and 8 GPU Tesla M2090 (6 GB per device), network is 1 Gb/s Ethernet.

- partition "tesla[21–30]": 10 CNs with two 6-cores CPU Intel Xeon X5675 (3.07 GHz), RAM is 192 GB, cache memory is 12 MB L3 cache and 8 GPU Tesla M2090 (6 GB per device), with network is Infiniband 20 Gb/s.
- partition "tesla[33–45]": 13 CNs with two 8-cores CPU Intel Xeon E5-2660 (2.2 GHz), cache memory is 20 MB L3 cache, RAM is 96 GB, and 8 GPU Tesla M2090 (6 GB per device), network is Infiniband 20 Gb/s.
- partition "tesla[48–52]": 5 CNs with two 8-cores CPU Intel Xeon E5-2650 (2.6 GHz), cache memory is 20 MB L3 cache, RAM is 64 GB and 3 GPU Tesla K40m (12 GB per device), network is Infiniband 20 Gb/s.

The results of comparing two algorithms of the conjugate gradient method on SLAEs containing test matrices are presented in Table 1. The results are given for several types of computing nodes using a single graphics accelerator.

Table 1. Statistics of the test problems. Problem names, dimensions (N), number of nonzeros (nnz), device type (DT) and problem analysis in terms of the timing in seconds.

Matrix	N	nnz	# iter.	DT	Time, s	
					CG	CGwO
Plat362	362	5786	991	M2090	6.88E-01	3.07E-01
				K40m	4.13E-01	3.12E-01
1138_bus	1138	4054	717	M2090	3.81E-01	1.84E-01
				K40m	5.31E-01	2.01E-01
				debug	6.82E-01	1.90E-01
Muu	7102	170134	12	M2090	2.64E-01	4.68E-03
				K40m	3.31E-01	4.55E-03
Кии	7102	340200	378	M2090	4.31E-01	1.31E-01
				K40m	4.39E-01	1.35E-01
Pres_Poisson	14822	715804	661	M2090	6.72E-01	3.13E-01
				K40m	6.346E-01	2.73E-01
Inline_1	503712	36816342	5642	M2090	4.74E + 01	5.17E + 01
				K40m	3.06E + 01	$3.37E{+}01$
Fault_639	638802	28614564	4444	M2090	$3.83E{+}01$	$4.32E{+}01$
				K40m	2.44E+01	2.77E + 01
				debug	2.44E + 01	2.77E + 01
thermal2	1228045	8580313	2493	M2090	$1.35E{+}01$	1.82E + 01
				K40m	8.33E+00	$1.18E{+}01$
G3_circuit	1585478	7660826	592	M2090	3.43E + 00	4.32E + 00
				K40m	1.94E+00	$2.92E{+}00$
Quenn_4147	4147110	399499284	8257	M2090	5.46E + 02	5.78E + 02
				K40m	3.55E+02	3.75E + 02

The matrices are ordered by increasing the order of the system of equations (N) and the number of nonzero elements (nnz). Bold indicates the best time to solve the system in each case. The pipelined algorithm CGwO showed a reduction in execution time on small SLAEs which are characterized by a small computing load, due to which a reduction in communications provides less time. Note that the classic CG algorithm was implemented based on CUBLAS, while the CGwO variant uses matrix and vector operations of its own GPU implementation.

For systems Inline_1 and Fault_639, the execution time of the pipeline algorithm is 10 and 13.5% longer than the block version of CG, which is associated with additional vector operations that are not blocked by reduced communications. With a decrease in the number of iterations, for example, for solving a large system with G3_circuit) with an approximately equal number of equations with thermal2, the execution time of the CG and CgwO algorithms on one GPU increases slightly. For the system (thermal2 and G3_circuit) the increase in costs becomes more significant.

Table 2 presents the results of the block variant of the algorithms for computing on several computing nodes for systems with small dimension matrices. Here are the results for 2 and 3 subdomains. Each subdomain was considered on a separate computing node. Communications were carried out using MPI technology. A significant influence of network characteristics on the performance of block methods can be seen in Table 2 for system of equations with matrix 1138_bus. Computations for these SLAEs were performed at various computing nodes with different throughput and latency of the network. In numerical experiments on the CNs (partition "debug") connected by a Gigabit network, communication costs significantly increase the execution time of the CG algorithm.

Matrix/DT	CG/#blocks		CGwO/#blocks		
	2	3	2	3	
Plat362/M2090	1.55E+00		1.22E + 00		
/K40m	1.92E+00	$1.56E{+}00$	$1.28E{+}00$	1.31E + 00	
1138_bus/M2090	1.84E + 00		9.28E-01		
/K40m	1.90E+00	$1.85E{+}00$	$1.03E{+}00$	1.04E + 00	
/debug	$1.25E{+}01$		$5.36\mathrm{E}{+00}$		
Muu/M2090	6.12E-01		2.29E-01		
/K40m	6.59E-01	5.64 E-01	2.89E-01	2.88E-01	
Kuu/M2090	1.30E + 00		6.43E-01		
$/{ m K40m}$	1.29E + 00	1.36E + 00	6.81E-01	7.95E-01	
$\tt Pres_Poisson/M2090$	1.55E+00		9.57E-01		
$/{ m K40m}$	1.60E + 00	1.66E + 00	$1.02E{+}00$	1.19E + 00	
${\tt G3_circuit}/{ m M2090}$	4.27E + 00		$3.99E{+}00$		
/K40m	4.04E+00	$3.510E{+}00$	3.27E + 00	$2.77\mathrm{E}{+00}$	

Table 2. Time of solving by the block algorithms CG and CGwO on CPU/GPU, s.

For example, in the variant 1138_bus on the cluster partition "debug", the execution time of the pipeline algorithm is 3.6 times less (the line "debug" in Table 2 and any row in Table 1). Using the Infiniband 20 Gb/s communication network reduces the execution time for all presented systems of equations (lines "M2090" and "K40m").

When reducing the computational load, a decrease in the number of synchronization points and the consolidation of transfers per transaction is more pronounced. This shows a comparison of systems with matrices Kuu and Muu. Both systems have an equal number of equations and nonzero elements, but the conditionality of these matrices is significantly different and, as a consequence, the number of iterations in the conjugate gradient method is different. Table 1 shows that using the pipeline algorithm for the matrix Muu gives speedup by 70 times, compared with the matrix Kuu, where the speedup is only 2.8.

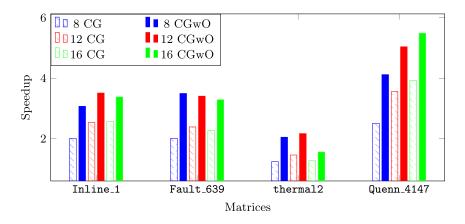


Fig. 1. Speedup of the block algorithms CG and CGwO

Figure 1 presents the results of accelerating the block algorithms of the conjugate gradient method, when divided into a larger number of blocks, accordingly 8, 12 and 16. To compute the speedup, parallel application was run repeatedly with different mapping of subdomains to several CPUs and GPUs. For example, in the case of 12 subdomains, variants were considered: 2 CPUs with 6 GPUs, 3 CPUs with 4 GPUs, 6 CPUs with 2 GPUs. The best time is shown.

The speedup was considered relative to the option on one GPU from Table 1. An application that implements this algorithm was executed in the exclusive mode of the computing node but not of the network.

As can be seen from the presented results, the pipelined CG shows the speedup greater than the classic version of conjugate gradient method. Wherein, for the largest of the considered matrices Quenn_4147, the speedup achieves 5.49 times, while the classical version gives 3.92 as maximum. For the strongly sparse matrix thermal2, block algorithms don't give high speedup (maximum is 1.56),

since the computational load depends mainly on the number of the nonzero elements.

An analysis of the results showed that reducing the data size due to the matrix partitioning and reducing the synchronization points slightly decrease the impact of communication costs on the total algorithm performance. Only the use of computing nodes connected by Infiniband allowed us to get speedup when computing on several computing nodes. The matrix partitioning into blocks allowed to decrease the execution time of the pipelined block algorithm in comparison with the conjugate gradients on one node on the matrices Inline_1, Fault_639 by reducing the computational load on one GPU.

Large systems thermal2, G3_circuit, solved by the block of the CGwO algorithm, as well as the reduction in communications costs and synchronization points, do not overlap the increasing costs of additional vector operations.

5 Conclusion

The heterogeneous computing platforms containing and sharing CPU + GPUs provide an effective solution to a wider range of problems with high energy efficiency when CPU and GPUs are uniformly loaded.

The parallel implementation of the solution of systems of linear algebraic equations on a heterogeneous platform was considered. The performance of parallel algorithms for classical conjugate gradient method is significantly limited by synchronization points when using the CPU and GPU together. A pipelined algorithm of the conjugate gradient method with one synchronization point was proposed. Also, it is provided the possibility of asynchronous computations, load balancing between several GPUs located both on the same computing node and for a GPU cluster when solving systems of large-dimensional equations. To further increase the efficiency of calculations, it is supposed to study not only the communication load of the algorithms but also the distributing of the computational load between the CPU and GPU. To obtain more reliable evaluation of communications costs, it is necessary to conduct a series of computational experiments on supercomputer with a completely exclusive mode of operation and a large number of heterogeneous nodes.

The following conclusions can be drawn from the analysis of data obtained during numerical experiments: the use of a pipeline algorithm reduces communication costs, but increases computational ones. For systems of small sizes or with a small number of iterations, this reduces the execution time of the algorithm when using a single GPU. For systems of large dimensions, a reduction in execution time, in comparison with CG, is possible only with a sufficiently small partition of the matrix into blocks, in which the increased computing costs overlap the communication decrease.

The proposed block algorithms, in addition to reducing the execution time, allow solving large linear systems that requires memory resources not provided by one GPU or computing node. At the same time, the pipelined block algorithm reduces the overall execution time by reducing synchronization points and combining communications into one message.

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